COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
BACHELOR OF COMPUTER APPLICATIONS (B.C.A)
II YEAR

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SYLLABUS PART - I

UNIT-I
Basic computer organization and design, Instructions and instruction codes, Timing and control/ instruction
cycle, Register/ Types of register/ general purpose & special purpose registers/ index registers, Register transfer
and micro operations/ register transfer instructions, Memory and memory function, Bus/ Data transfer
instructions, Arithmetic logic micro-operations/ shift micro-operations, Input/ Output and interrupts, Memory
reference instructions, Memory interfacing , Cache memory.
UNIT-II
Central Processing Unit
General Register Organization/ stacks organizations, instruction formats, addressing modes, Data transfer and
manipulation. Program control, reduced computer, pipeline/ RISC/ CISC pipeline vector processing/ array
processing.
Arithmetic Algorithms: Integer multiplication using shift and add, Booth's algorithm,
Integer division, Floating-point representations.

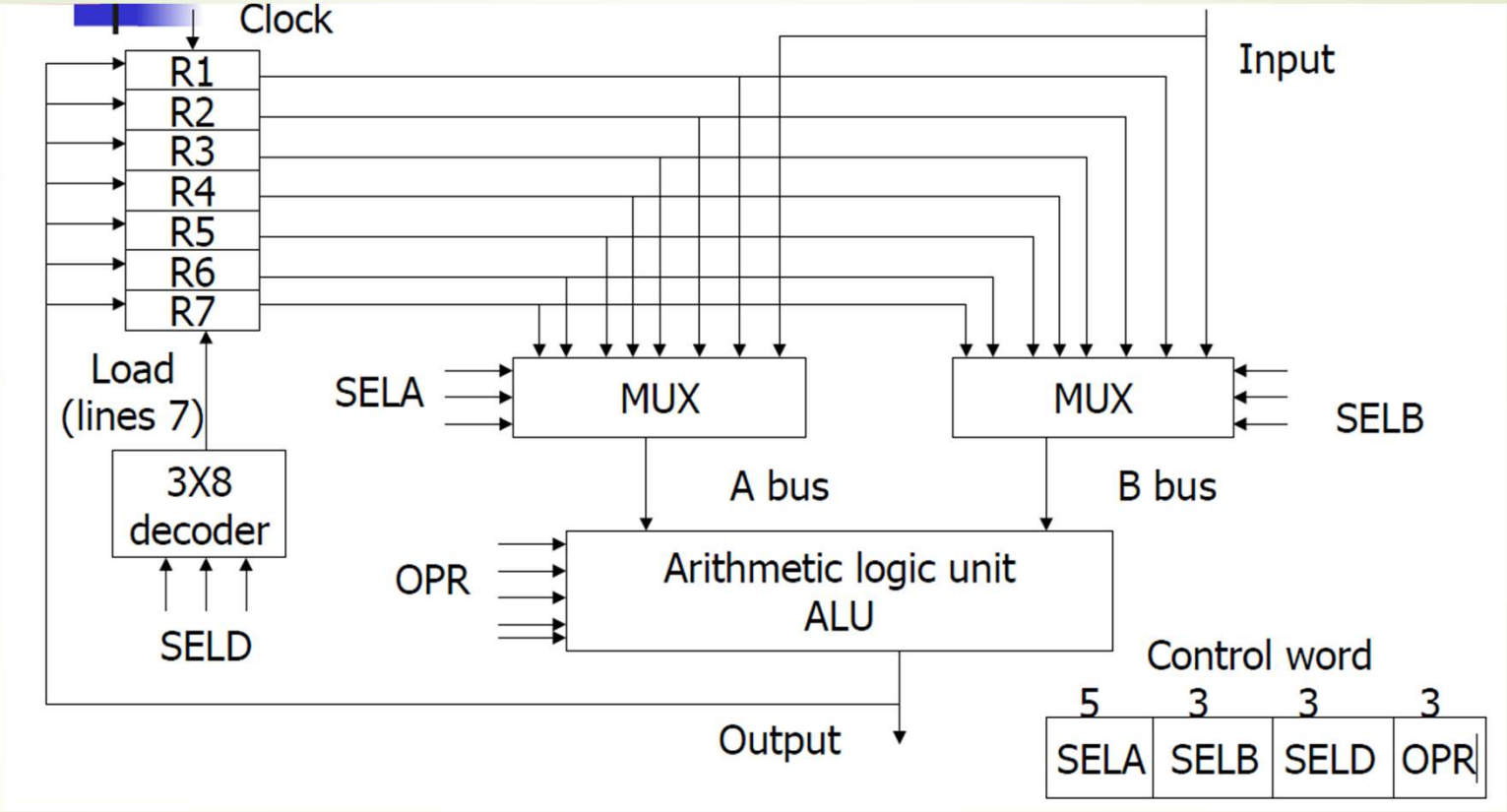
SYLLABUS PART - II

UNIT-III
Computer Arithmetic
Addition, subtraction and multiplication algorithms, divisor algorithms. Floating point, arithmetic operations,
decimal arithmetic operations.
UNIT-IV
Input – Output Organization
Peripheral devices, Input/output interface, ALU Asynchronous Data transfer, mode of transfer, priority interrupts, Direct memory Address (DMA), Input/ Output processor (IOP), serial communication.
UNIT-V
Evaluation of Microprocessor
Overview of Intel 8085 to Intel Pentium processors, Basic microprocessors, architecture and interface, internal
architecture, external architecture memory and input/ output interface.
UNIT-VI
Assembly language, Assembler, Assembly level instructions, macro, use of macros in I/C instructions, program
loops, programming arithmetic and logic subroutines, Input-Output programming.

MODULE - I

CENTRAL PROCESSING UNIT

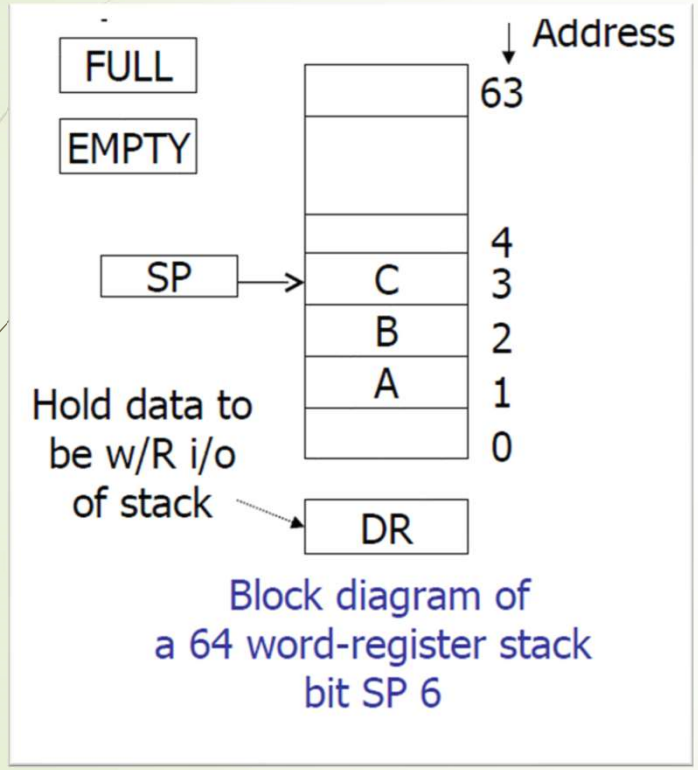
General Register Organization



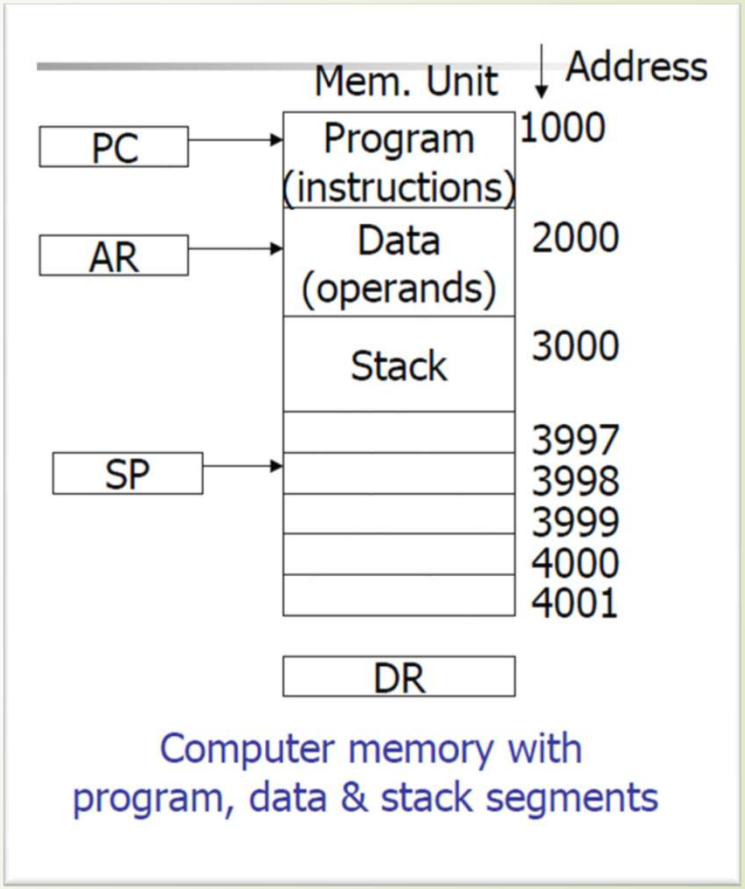
Stack Organization

- The stack in digital computers is essentially a memory unit with an address register (Stack Pointer SP) that count only after an initial value is loaded into the stack.
- SP value always point at the top item in the stack.
- The 2 operations of stacks are the insertion (push), and deletion (pop) of items.
- A stack can be organized as a collection of a finite number of memory words or registers.
- In a 64-word stack, SP contains 6 bits because $2^6 = 64$.
- The 1-bit register FULL is set to 1 when stack is full.
- The 1-bit register EMTY is set to 1 when stack is empty.
- DR is data register that holds the binary data to be written into or read out of the stack.

Stack Organization



Block diagram of
a 64 word-register stack
bit SP 6



Computer memory with
program, data & stack segments

INSTRUCTION FORMATS

- The bits of the instruction are divided into groups called fields.
- The most common fields founded in the instruction formats are:
  - An operation code field
  - An address field.
  - A mode field
- Data executed by instructions (operands) are stored either in memory or in processor registers.
- Operands residing in memory are specified by their memory address.
- Operands residing in registers are specified with a register address.
- A register address is binary number of k bits that defines one of 2^K registers in the CPU.
- Most computers fall into one of the 3 types of CPU organizations:
  - Single Accumulator (AC) Organization, i.e. ADD X
  - General register (Rs) Organization, ADD R1,R2,R3
  - Stack Organization, i.e. ADD (pop and add 2 operand then push the result into the stack)
- Some computers combine features from more than one organization structure, Ex. Intel 8080 (GRs for register transfer, AC used in arithmetic operations)

ADDRESSING MODES

Instruction format with mode field

Opcode	Mode	Address

- A register address is binary number of k bits that defines one of 2^k registers in the CPU.
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  - General register (Rs) Organization, ADD R1,R2,R3
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- Some computers combine features from more than one organization structure, Ex. Intel 8080 (GRs for register transfer, AC used in arithmetic operations)
- Other computers use a single binary for operation & Address mode.
- The mode field is used to locate the operand.
- Address field may designate a memory address or a processor register.
- There are 2 modes that need no address field at all (Implied & immediate modes).

ADDRESSING MODES LISTED

- Implied mode.
- Immediate mode
- Register mode
- Register Indirect mode
- Auto-increment or Auto-decrement mode
- Direct Mode
- Indirect Mode
- Relative Address Mode
- Index Addressing Mode

Data Transfer

- Data transfer instructions cause transfer of data from one location to another without changing the binary information. The most common transfer are between the:
  - Memory and Processor registers
  - Processor registers and input output devices
  - Processor registers themselves

Data Transfer Instructions

- **Load(LD)** : transfer from memory to a processor register, usually an AC (*memory read*)
- **Store(ST)** : transfer from a processor register into memory (*memory write*)
- **Move(MOV)** : transfer from one register to another register
- **Exchange(XCH)** : swap information between two registers or a register and a memory word
- **Input/Output(IN/OUT)** : transfer data among processor registers and input/output device
- **Push/Pop(PUSH/POP)** : transfer data between processor registers and a memory stack

DATA MANIPULATION INSTRUCTIONS

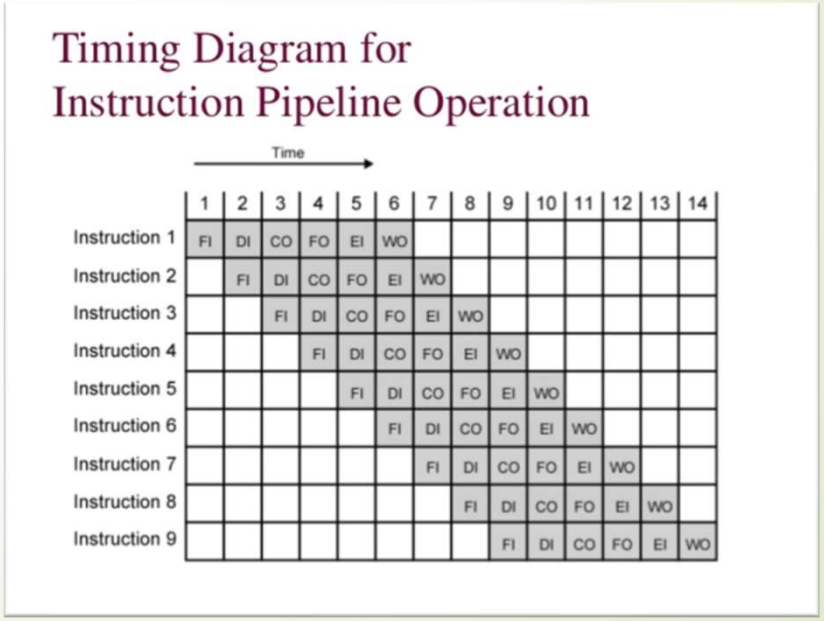
- The data manipulation instructions in a typical computer are usually divided into three basic types:
  - Arithmetic instructions
  - Logical and bit manipulation instructions
  - Shift instructions

✓ Arithmetic Instructions :The four basic arithmetic operations are addition, subtraction, multiplication and division. Most computers provide instructions for all four operations

Name	Mnemonic
Increment	INC
Decrement	DEC
Add	ADD
Subtract	SUB
Multiply	MUL
Divide	DIV
Add with carry	ADDC
Subtract with borrow	SUBB
Negate (2's complement)	NEG

PIPELINE

- In computing, a **pipeline**, also known as a data **pipeline**, is a set of data processing elements connected in series, where the output of one element is the input of the next one. The elements of a **pipeline** are often executed in parallel or in time-sliced fashion.



RISC / CISC

- **Reduced Set Instruction Set Architecture (RISC) –**
  The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating and storing operations just like a load command will load data, store command will store the data.
- **Complex Instruction Set Architecture (CISC) –**
  The main idea is that a single instruction will do all loading, evaluating and storing operations just like a multiplication command will do stuff like loading data, evaluating and storing it, hence it's complex.
- Both approaches try to increase the CPU performance
  - **RISC:** Reduce the cycles per instruction at the cost of the number of instructions per program.
  - **CISC:** The CISC approach attempts to minimize the number of instructions per program but at the cost of increase in number of cycles per instruction.

CHARACTERISTICS

- **Characteristic of RISC –**

1. Simpler instruction, hence simple instruction decoding.
2. Instruction come under size of one word.
3. Instruction take single clock cycle to get executed.
4. More number of general purpose register.
5. Simple Addressing Modes.
6. Less Data types.
7. Pipeling can be achieved.

- **Characteristic of CISC –**

1. Complex instruction, hence complex instruction decoding.
2. Instruction are larger than one word size.
3. Instruction may take more than single clock cycle to get executed.
4. Less number of general purpose register as operation get performed in memory itself.
5. Complex Addressing Modes.
6. More Data types.

Excercises

- Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in signed-l's complement representation.
- Prove that the multiplication of two n-digit numbers in base r gives a product no more than 2n digits in length. Show that this statement implies that no overflow can occur in the multiplication operation.
- Show the contents of registers E, A, Q, and SC (as in Table 10-2) during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included.
- Show the contents of registers E, A, Q, and SC (as in Fig. 10-12) during the process of division of (a) 10100011 by 1011; (b) 00001111 by 0011 . (Use a dividend of eight bits.)
- Show that there can be no mantissa overflow after a multiplication operation.
- Show that the division of two normalized floating-point numbers with fractional mantissas will always result in a normalized quotient provided a dividend alignment is carried out prior to the division operation.
- Show the hardware to be used for the addition and subtraction of two decimal numbers in signed-magnitude representation. Indicate how an overflow is detected.
- Show that 673 - 356 can be computed by adding 673 to the 10's complement of 356 and discarding the end carry. Draw the block diagram of a three-stage
- Decimal arithmetic unit and show how this operation is implemented. List all input bits and output bits of the unit.

Reference

- Reference Books:
- 1. Leventhal, L.A, “Introduction to Microprocessors”, Prentice Hall of India
- 2. Mathur, A.P., “Introduction to Microprocessors”, Tata McGraw Hill
- 3. Rao, P.V.S., “Prospective in Computer Architecture” , Prentice Hall of India

Declaration

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THANK YOU!!!